PUB-NO: JP410335195A
DOCUMENT-IDENTIFIER: JP 10335195 A
TITLE: PRODUCTION OF PASTED BOARD

PUBN-DATE: December 18, 1998

INVENTOR-INFORMATION:

NAME	COUNTRY
TANIGUCHI, TORU	
MORITA, ETSURO	

INT-CL (IPC): H01 L 21/02; H01 L 21/304; H01 L 21/304; H01 L 27/12

ABSTRACT:

PROBLEM TO BE SOLVED: To prevent generation of voids between wafers by beveling the outer circumferential part on one side of a wafer through etching thereby enhancing smoothness at the outer circumferential edge on the surface of the wafer.

SOLUTION: A masking disc 3 smaller than a wafer 1 for active layer is pasted to the surface thereof with the outer circumference of the wafer being exposed. A plurality of wafers 1 for active layer are then laminated sequentially while superposing the masking discs 3 each other thus forming a laminate 4. Subsequently, the circumferential edge parts of respective wafers 1 for active layer are immersed collectively into an etching liquid of HF/HNO3 while turning the laminate 4 about the axis (a) of the wafer at a specified speed thus beveling the wafers 1 through etching. Since mechanical beveling process can be eliminated after pasting the wafers, machining damage due to mechanical beveling is eliminated and the outer circumferential part of the wafer for active layer is protected against damage on the surface side thereof.

DERWENT-ACC-NO: 1999-111902
DERWENT-WEEK: 199910

1026-(12)-(13)

TITLE: Laminated substrate manufacture for SOI substrate manufacture - involves forming masking material by exposing periphery of single side of wafer for barrier layers and etching it subsequently using etching liquid

PRIORITY-DATA: 1997JP-0154501 (May 27, 1997)

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PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	JP 10335195 A	December 18, 1998		006	H01L021/02

INT-CL (IPC): H01 L 21/02; H01 L 21/304; H01 L 27/12

ABSTRACTED-PUB-NO: JP 10335195A
BASIC-ABSTRACT:

NOVELTY - A masking material (3) is formed on the periphery of single side of a wafer (1) for barrier layers by exposing it. The etching bevelling of periphery of wafer for barrier layer is performed by using etching liquid (5) due to which the mask material is removed. The surface outside etched area is heat treated and is laminated to wafer for support substrate. Then, the bevelled area of barrier layer wafer periphery is ground and polished.

USE - For SOI substrate manufacture.

ADVANTAGE - The damage to the surface side of periphery of wafer for support substrate is prevented. The smoothness in the surface of wafer for barrier layers is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the etching bevelling process of wafer periphery. (1) Wafer; (3) Masking material; (5) Etching liquid.

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平10－335195

(43)公開日　平成10年(1998)12月18日

(51)Int.Cl.[6]		識別記号	FI		
H01L	21/02		H01L	21/02	B
	21/304	301		21/304	301B
		321			321M
	27/12			27/12	B

審査請求　未請求　請求項の数2　ＦＤ　（全 6 頁）

(21)出願番号　特願平9－154501

(22)出願日　平成９年(1997)５月27日

(71)出願人　000228925
三菱マテリアルシリコン株式会社
東京都千代田区大手町一丁目５番１号

(72)発明者　谷口　徹
東京都千代田区大手町１丁目５番１号　三菱マテリアルシリコン株式会社内

(72)発明者　森田　悦郎
東京都千代田区大手町１丁目５番１号　三菱マテリアルシリコン株式会社内

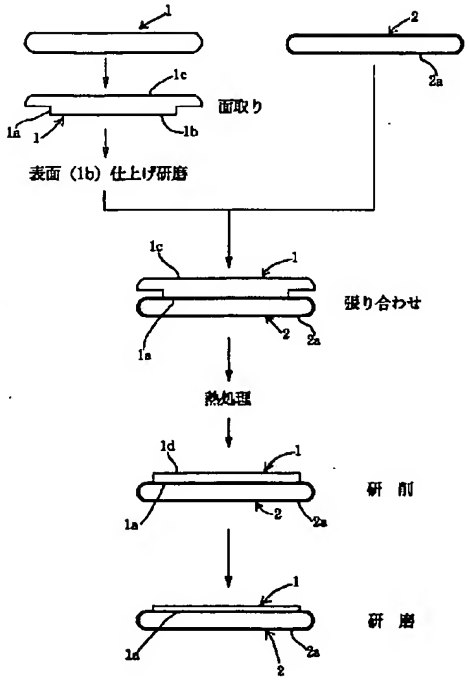
(74)代理人　弁理士　安倍　逸郎

(54)【発明の名称】　張り合わせ基板の製造方法

(57)【要約】

【課題】　活性層用ウェーハの表面外周縁の平滑性を向上してボイド発生を防止し、張り合わせ熱処理時のスリップ発生を防止する。エッチング時に支持基板用ウェーハの小径化が起きない張り合わせ基板の製造方法を提供する。

【解決手段】　活性層用ウェーハ１の表面に、ウェーハ外周部を露呈した状態でマスキング材３を貼着する。マスキング材３同士を重ね合わせながら、活性層用ウェーハ１を順次積層して積層体４を形成する。これをウェーハ軸線ａを中心に回転しつつ、それぞれの活性層用ウェーハ１のウェーハ周縁部をエッチング液５に浸漬してエッチング面取りする。この結果、ウェーハ１の表面外周縁の平滑性が向上し、ボイド発生、スリップ発生を防止できる。しかも、ウェーハ外周部のエッチング時に支持基板用ウェーハの小径化が生じない。この後、表面仕上げ研磨を施して張り合わせ、熱処理後、研削、研磨する。



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【特許請求の範囲】
【請求項１】　支持基板用ウェーハと活性層用ウェーハとを張り合わせた張り合わせ基板の製造方法において、
上記活性層用ウェーハの片面に、そのウェーハ外周部を露呈してマスキング材を設ける工程と、
このマスキング材を有する活性層用ウェーハをエッチング液に接触させて、上記ウェーハ片面の外周部をエッチング面取りする工程と、
上記マスキング材を除去する工程と、
上記面取り側の面を張り合わせ面として、上記活性層用ウェーハを上記支持基板用ウェーハに張り合わせ、その後に熱処理する工程と、
上記張り合わせ後の活性層用ウェーハの表面を、上記ウェーハ外周部の面取り部分に達するまで研削する工程と、
この研削面を研磨する工程とを備えた張り合わせ基板の製造方法。
【請求項２】　上記マスキング材を設けた後、該マスキング材同士を重ね合わせながら、複数枚の上記活性層用ウェーハを順次積層し、次いでこの積層体をウェーハ軸線を中心に回転しつつ、各ウェーハ周縁部を一括してエッチング液に浸すことによりエッチング面取りする請求項１に記載の張り合わせ基板の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は張り合わせ基板の製造方法、例えばシリコンｏｎシリコン基板（直接張り合わせ基板）、間に絶縁層を介在させたＳＯＩ（Ｓｉｌｉｃｏｎ　ｏｎＩｎｓｕｌａｔｏｒ）基板などの張り合わせ基板の製造方法に関する。
【０００２】
【従来の技術】ＳＯＩ基板の製造では、絶縁膜（SiO_2）を挟んで支持基板用シリコンウェーハと活性層用シリコンウェーハとを室温で重ね合わせ、その後、所定の張り合わせ熱処理を行っている。さらに、張り合わせ不良領域を除去するため、活性層用ウェーハの外周部を面取りしている。その後、活性層用ウェーハの表面を研削し、研磨している。
【０００３】この張り合わせ後の面取りは、具体的には、活性層用ウェーハの外周部を面取り用ホイールによって研削し、その後、この面取り面をエッチングして加工ダメージを除去するのが通常である。この加工ダメージの除去方法としては、図４に示すように、張り合わせ基板を多数ギャザーしてのディッピングによるエッチングが知られている。このギャザーエッチングでは、活性層用ウェーハ１００の表面１００ａ同士を重ね合わせながら、所定枚数の張り合わせ基板１０１を順次積層する。その後、この積層体１０２をウェーハ軸線ａを中心に回転しつつ、各ウェーハ周縁部を一括してエッチング液１０３に浸す。この張り合わせ後のウェーハ外周部の

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面取りでは、ホイールを用いて機械的面取りを施す際に、加工ダメージが支持基板用ウェーハ１０４の表側へも及ぶという問題点があった。なお、図４は従来手段に係るギャザーディッピングによる張り合わせ基板のエッチング工程を示す説明図である。同図において、１０４は支持基板用ウェーハ、１０４ａは支持基板用ウェーハ１０４の表面に形成されたSiO_2膜である。
【０００４】そこで、これを解消する従来技術として、例えば特開平４－８５８２７号公報に記載の「半導体装置の製造方法」が知られている。この従来方法は、張り合わせ前に、活性層用ウェーハの外周部に対して、砥石であるホイールにより機械的面取りを施すものである。なお、その後は、この面取り側の面を張り合わせ面にして、活性層用ウェーハと支持基板用ウェーハとを張り合わせ、所定の熱処理後、活性層用ウェーハの表面に研削、研磨等を施す。
【０００５】また、これとは別の従来技術として、例えば特開平３－２５０６１６号公報に記載された「接合ウェーハ及びその製造方法」が知られている。この別方法は、ウェーハ同士を張り合わせ後、エッチング面取りにより活性層用ウェーハの外周部を除去するものである。以下、これを、図５の他の従来手段に係るギャザーディッピングによる張り合わせ基板のエッチング工程を示す説明図を参照して説明する。
【０００６】同図において示すように、活性層用ウェーハ２００を中間にSiO_2膜を介して支持基板用ウェーハ２０１に張り合わせて張り合わせ基板２０２を作製する。これらの張り合わせ基板２０２では、それぞれ、その活性層用ウェーハ２００を表面研削する。その後、各活性層用ウェーハ２００の外周部以外の表面にマスキングテープ２０３を貼着する。次に、マスキングテープ２０３の表面同士を重ね合わせて、これらの多数枚の張り合わせ基板２０２をギャザーする。その後、この積層体２０４をエッチング液２０５にディッピングし、各活性層用ウェーハ２００の外周部をエッチング除去する。
【０００７】
【発明が解決しようとする課題】しかしながら、これらの従来の方法では、以下の不都合があった。すなわち、図６に示すように、前者の張り合わせ前、活性層用ウェーハ３００の外周部にホイール３０１による機械的面取りを施すものの場合には、研削用のホイール３０１は、度重なる面取り加工によりその研削面３０１ａが荒れているのが通常である。このような荒れた研削面３０１ａによる機械的面取りの結果、図７（ａ）、図７（ｂ）に示すように、活性層用ウェーハ３００の面取り部分の内周側部３００ｂが荒くなり、活性層用ウェーハ３００の表面３００ｃの外周縁に加工ダメージが生じるおそれがあった。よって、この加工ダメージを原因としてウェーハ間にボイドが発生するという問題点があった。また、活性層用ウェーハ３００の面取り部分の内周側部３００

bに生じた研削の加工ダメージが比較的大きい場合には、張り合わせ後の熱処理時に、このダメージに起因するスリップが生じるという問題点もあった。なお、図6は従来手段に係る活性層用ウェーハ外周部の機械的面取り工程の説明図、図7（a）は従来手段に係る機械的面取り後の活性層用ウェーハの外周部の拡大断面図、図7（b）は同じくそのウェーハ外周部の拡大平面図である。

【0008】一方、図5に示すように、張り合わせ後、活性層用ウェーハ200の外周部にマスキングテープ202を用いたエッチング面取りを施すものの場合には、活性層用ウェーハ200の外周部だけでなく、支持基板用ウェーハ201の外周部も、そのウェーハ厚さ全域にわたってエッチング除去されるので、支持基板用ウェーハ201が小径化するという問題点があった。

【0009】

【発明の目的】そこで、この発明は、面取りされた活性層用ウェーハの表面の外周縁における平滑性を向上でき、これによりウェーハ間のボイド発生を防止できる張り合わせ基板の製造方法を提供することを、その目的としている。また、この発明は、張り合わせ熱処理時に、面取りによる加工ダメージに起因した活性層用ウェーハのスリップ発生を防止できる張り合わせ基板の製造方法を提供することを、その目的としている。さらに、この発明は、エッチング面取りによる支持基板用ウェーハの小径化が起きない張り合わせ基板の製造方法を提供することを、その目的としている。さらまた、外周部がエッチング面取りされた活性層用ウェーハを大量生産可能な張り合わせ基板の製造方法を提供することを、その目的としている。

【0010】

【課題を解決するための手段】請求項1に記載の発明は、支持基板用ウェーハと活性層用ウェーハとを張り合わせた張り合わせ基板の製造方法において、上記活性層用ウェーハの片面に、そのウェーハ外周部を露呈してマスキング材を設ける工程と、このマスキング材を有する活性層用ウェーハをエッチング液に接触させて、上記ウェーハ片面の外周部をエッチング面取りする工程と、上記マスキング材を除去する工程と、上記面取り側の面を張り合わせ面として、上記活性層用ウェーハを上記支持基板用ウェーハに張り合わせ、その後に熱処理する工程と、上記張り合わせ後の活性層用ウェーハの表面を、上記ウェーハ外周部の面取り部分に達するまで研削する工程と、この研削面を研磨する工程とを備えた張り合わせ基板の製造方法である。

【0011】ここでいうマスキング材とは、テフロン（商品名；フッ素樹脂）、ポリエチレンなどの合成樹脂からなるマスキングテープや、耐蝕性に優れたワックス、その他の高分子有機化合物などからなる皮膜でもよい。マスキング材の厚さは、80μm以上が好ましく、

80μm未満では例えばマスキング材同士を重ね合わせて積層体を形成し、これの各ウェーハ周縁部を一括してエッチング液に浸してエッチング面取りする際に、このエッチング液が、隣接する活性層用ウェーハの外周部同士の隙間へ入り込みにくい。また、ここでいうエッチング面取りとは、例えばフッ酸と硝酸とを混合した混酸、水酸化カリウムまたは水酸化ナトリウムなどのエッチング液中に、例えば活性層用ウェーハを所定時間（HF／HNO_3では3～5分間）だけ接触させ、これによりマスキング材で被われていない活性層用ウェーハの外周部を所定量だけ溶失させることをいう。

【0012】さらに、活性層用ウェーハの外周部の好ましいエッチング面取りによる厚さは、50μm～ウェーハの厚さの1／2である。50μm未満では、活性層用ウェーハと支持基板用ウェーハとの張り合わせ後の活性層用ウェーハの表面研削時に、支持基板用ウェーハの周縁部の表面側を傷つけるおそれがある。一方、ウェーハ厚さの1／2を超えると、ウェーハ外周部の機械的強度が大幅に低下するおそれがある。

【0013】活性層用ウェーハの外周部の半径方向のエッチング面取り幅は、0．8～5．0mm、特に1～3mmが好ましい。0．8mm未満では各ウェーハの外周研磨だれに起因する接合不良が起き易くなる。また、5．0mmを超えるとウェーハでの有効エリアが小さくなる。また、張り合わせ後の活性層用ウェーハの表面の研削厚さは、少なくとも面取り部分に達していればよく、限定されない。

【0014】さらに、活性層用ウェーハは、支持基板用ウェーハに張り合わされる前に、張り合わせ面の表面仕上げ研磨を行ってもよい。ここでいう表面仕上げ研磨とは、表面基準のワックスレス研磨で0．1μm未満の研磨をいう。活性層用ウェーハの表面仕上げ研磨後は、通常、SC1（Standard Cleaning 1）、SC1＋希塩酸、SC1＋HCl／HF、SC1＋HFなどによる活性層用ウェーハの表面の洗浄を行う。なお、活性層用ウェーハとしては、その表面がSiO_2膜により被われているものであってもよい。また、このSiO_2膜は、張り合わせ基板の製造工程中、どの工程で活性層用ウェーハに設けてもよい。

【0015】請求項2に記載の発明は、上記マスキング材を設けた後、該マスキング材同士を重ね合わせながら、複数枚の上記活性層用ウェーハを順次積層し、次いでこの積層体をウェーハ軸線を中心に回転しつつ、各ウェーハ周縁部を一括してエッチング液に浸すことによりエッチング面取りする請求項1に記載の張り合わせ基板の製造方法である。活性層用ウェーハの積層枚数や回転速度は、張り合わせ基板を多数ギャザーし、ディッピングによりエッチングする従来方法と、基本的に同じである。なお、活性層用ウェーハのエッチング面取りは、このように複数枚一括して行わなくても、1枚ずつ行って

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もよい。

【００１６】

【作用】この発明によれば、支持基板用ウェーハに張り合わせる前に、予め活性層用ウェーハの片面に、ウェーハ外周部を露呈してマスキング材を設け、その後、このマスキング材付きの活性層用ウェーハをエッチング液に浸して、活性層用ウェーハの片面の外周部をエッチングにより面取りする。次いで、面取り側の面を張り合わせ面にして、活性層用ウェーハと支持基板用ウェーハとを張り合わせ、その後熱処理する。それから、張り合わせ後の活性層用ウェーハの表面を面取り部分に達するまで研削し、さらにこの研削面を研磨して張り合わせ基板を製造する。

【００１７】従来におけるウェーハ外周部の面取りでは、張り合わせ後における機械的面取り（砥石での面取り）か、エッチング面取りが採用されていた。この結果、支持基板用ウェーハの外周部の表面側をこの砥石により傷つけたり、支持基板用ウェーハの外周部の一部がエッチング液に溶けて、エッチング面取りによる支持基板用ウェーハの小径化が生じるおそれがあった。しかしながら、この発明では、張り合わせ前にウェーハ外周部の面取りを行うので、これらのおそれがない。

【００１８】また、従来の機械的面取りの場合では、活性層用ウェーハにおける面取り部の内周側部は、通常、砥石であるホイールの、度重なる使用により荒れた研削面で研削される。このため、面取りされた活性層用ウェーハの表面の外周縁には、機械的面取りに起因する加工ダメージが発生した。しかしながら、この発明では、ホイールを用いずにエッチング液に浸して面取りするので、このような加工ダメージが発生せず、この結果、活性層用ウェーハの表面おける平滑性を向上できる。また、この面取りがエッチングによる面取りであるので、張り合わせ熱処理時において、面取りによる加工ダメージに起因した活性層用ウェーハのスリップ発生を防止できる。

【００１９】特に、請求項２に記載の発明によれば、まず複数枚ある活性層用ウェーハの片面にそれぞれマスキング材を設ける。その後、マスキング材同士を重ね合わせて活性層用ウェーハを順次積層する。次いで、この積層体をウェーハ軸線を中心に回転しつつ、各ウェーハ周縁部を一括してエッチング液に浸したり、エッチング液をスプレーすることにより、この部分をエッチング面取りする。この結果、外周部がエッチング面取りされた活性層用ウェーハを、比較的容易に大量生産できる。また、エッチングに際してのマスキング材の剥がれを完全になくすこともできる。

【００２０】

【発明の実施の形態】以下、この発明の実施例を図面を参照して説明する。なお、ここでは張り合わせ基板として、ＳＯＩ基板を例に説明する。図１は、この発明の一

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実施例に係る張り合わせ基板の製造方法のフローシートである。図２は、活性層用ウェーハの外周部のエッチング面取り工程を示す説明図である。図３は、エッチング面取り直後の活性層用ウェーハの拡大図である。

【００２１】この実施例によれば、図１に示すように、予めシリコン製の活性層用ウェーハ１（鏡面研磨ウェーハ）を用意する。また、活性層用ウェーハ１と同一素材および同一口径の支持基板用ウェーハ２（鏡面研磨ウェーハ）の表面に、絶縁膜である酸化膜（SiO_2）２ａを形成しておく。次に、活性層用ウェーハ１の外周部を表面側から、ウェーハ半径方向へ３ｍｍ、厚さ１００μｍだけエッチング面取りする。

【００２２】図２を参照してこのエッチング面取りを説明する。この活性層用ウェーハ１の表面に、ウェーハ外周部を露呈した状態で、このウェーハ１より小円板の日東電工株式会社製のマスキングテープ「ＢＴ－５０Ｅ」からなるマスキング材３を貼着する。その後、マスキング材３同士を重ね合わせながら、複数枚の活性層用ウェーハ１を順次積層して積層体４を形成する。次いで、積層体４をウェーハ軸線ａを中心に所定速度で回転しつつ、それぞれの活性層用ウェーハ１のウェーハ周縁部を一括してHF/HNO_3のエッチング液５に浸漬してエッチング面取りするものである。

【００２３】図３に示すように、このエッチング面取りにより、活性層用ウェーハ１のウェーハ外周部が厚さｔ（ここでは１００μｍ）だけ溶失した。なお、この溶失は活性層用ウェーハ１の外周部全体に及ぶ（図３二点鎖線参照）。このように、張り合わせ前に活性層用ウェーハ１の外周部の面取りを行うので、従来技術における張り合わせ後の機械的面取りの場合のように、支持基板用ウェーハ２の外周部の表面側を砥石により傷つけるおそれがない。とともに、エッチング時に支持基板用ウェーハ２の外周部が溶けて、このウェーハ２が小径化することもない。しかも、面取りされた活性層用ウェーハの表面の外周縁には、機械的面取りに起因する加工ダメージが生じていないので、活性層用ウェーハの表面における平滑性を向上できる。さらには、張り合わせ熱処理時において、面取りによる加工ダメージに起因した活性層用ウェーハ１のスリップを防止できる。

【００２４】その後、マスキング材３を剥がす。次に、図１に示すように、張り合わせ前の活性層用ウェーハ１の表面１ｂを仕上げ研磨する。仕上げ研磨は、表面基準のワックスレスマウント方式による０．１μｍ未満の研磨である。研磨後は、この活性層用ウェーハの表面の洗浄を行う。通常、ＳＣ１洗浄、ＳＣ１洗浄＋希塩酸洗浄、ＳＣ１洗浄＋ＨＦ洗浄、または、ＳＣ１洗浄＋ＨＣｌ／ＨＦ洗浄による。

【００２５】次いで、面取り側の表面１ｂを張り合わせ面として、活性層用ウェーハ１と支持基板用ウェーハ２とを室温で張り合わせる。さらに、所定の張り合わせ熱

処理を行う（例えば１１００℃、２時間）。この結果、支持基板用ウェーハ２に活性層用ウェーハ１が酸化膜２ａを介して張り合わされることとなる。その後、活性層用ウェーハ１を表面１ｃ側から面取り部分に達するまで比較的低番手の砥粒を有する図外のホイールにより粗研削する。次いで、活性層用ウェーハ１の外周部の残厚が目的厚さ＋５μｍとなるまで、比較的高番手の砥粒を有するホイールにより細研削する。次いで、この表面研削後の表面１ｄを５μｍだけ研磨する。これにより所定厚さ（例えば１０μｍ）の活性層が支持基板用ウェーハ２上に絶縁膜２ａを介して配設されたＳＯＩ基板が得られる。

【００２６】

【発明の効果】この発明に係る張り合わせ基板の製造方法によれば、支持基板用ウェーハとの張り合わせ前に、活性層用ウェーハの片面の、マスキング材により被覆されていない外周部をエッチング面取りするようにしたので、面取り時にベースとなる支持基板用ウェーハの外周部の表面側を傷つけるおそれがなくなるとともに、エッチング面取りによる支持基板用ウェーハの小径化が起きない。しかも、面取りされた活性層用ウェーハの表面の外周縁には、機械的面取りに起因する加工ダメージが生じることがない。この結果、活性層用ウェーハの表面における平滑性を向上できる。さらに、張り合わせ熱処理時において、この機械的面取り部分の加工ダメージに起因した活性層用ウェーハのスリップ発生も防止できる。そして、張り合わせ前にマスキング材をウェーハ表面に貼着しエッチングするため、工程数が増加することがなく、生産効率を高めることができる。

【００２７】特に、請求項２に記載の発明によれば、マスキング材付きの複数枚の活性層用ウェーハをマスキング材同士を重ね合わせて順次積層し、得られた積層体をウェーハ軸線を中心に回転しつつ、各ウェーハ周縁部を一括してエッチング液に浸してエッチング面取りするようにしたので、外周部がエッチング面取りされた活性層用ウェーハを、比較的容易に大量生産できる。

【図面の簡単な説明】

【図１】この発明の一実施例に係る張り合わせ基板の製造方法の概略を示すフローシートである。

【図２】この発明の一実施例に係る活性層用ウェーハの外周部のエッチング面取り工程を示す説明図である。

【図３】この発明の一実施例に係る活性層用ウェーハの外周部のエッチング面取り工程を示す説明図である。

【図４】従来手段に係るギャザーディッピングによる張り合わせ基板のエッチング工程を示す説明図である。

【図５】他の従来手段に係るギャザーディッピングによる張り合わせ基板のエッチング工程を示す説明図である。

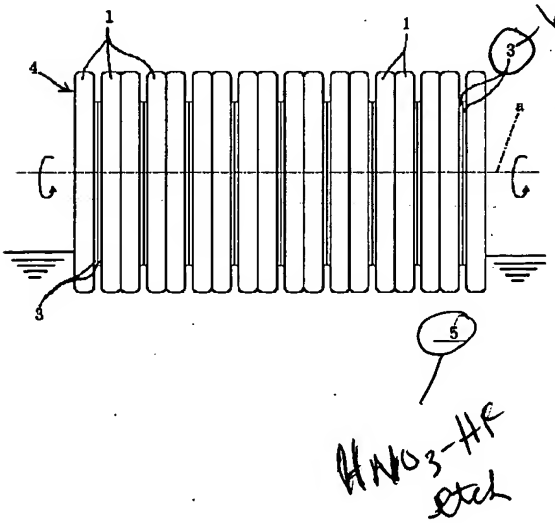
【図６】従来手段に係る活性層用ウェーハ外周部の機械的面取り工程の説明図である。

【図７】（ａ）は従来手段に係る機械的面取り後の活性層用ウェーハの外周部の拡大断面図である。（ｂ）は同じくそのウェーハ外周部の拡大平面図である。

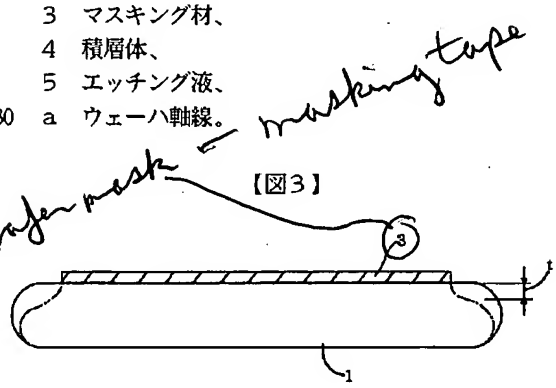
【符号の説明】

１　活性層用ウェーハ、
２　支持基板用ウェーハ、
３　マスキング材、
４　積層体、
５　エッチング液、
ａ　ウェーハ軸線。

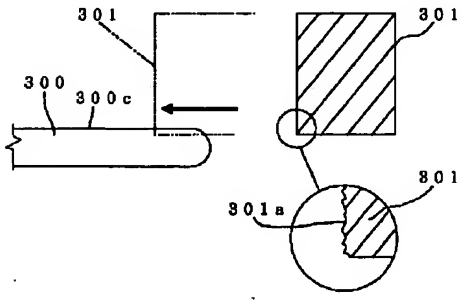
【図２】



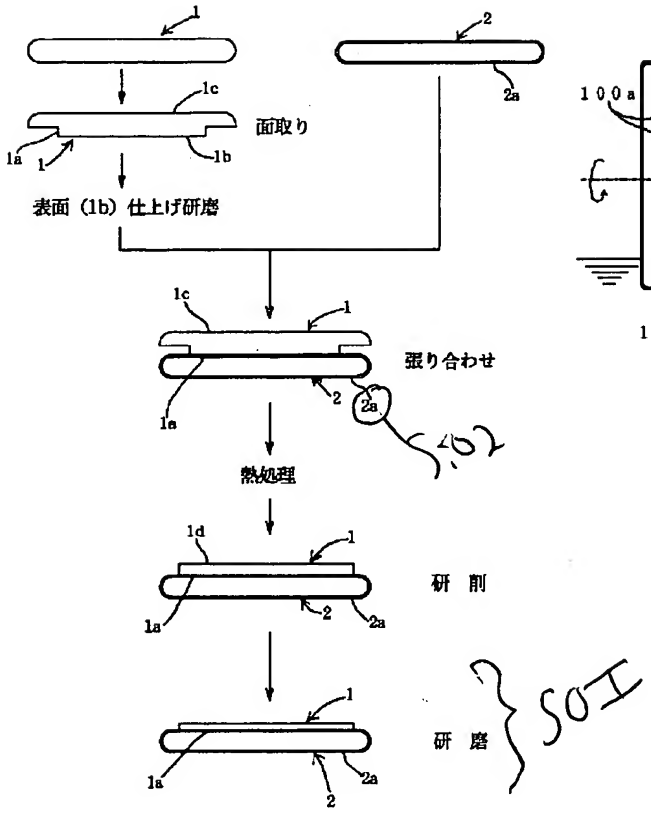
【図３】



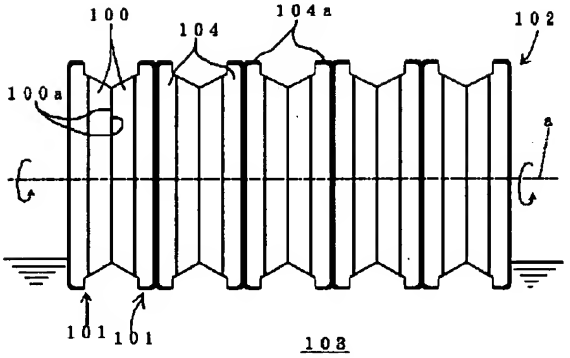
【図６】



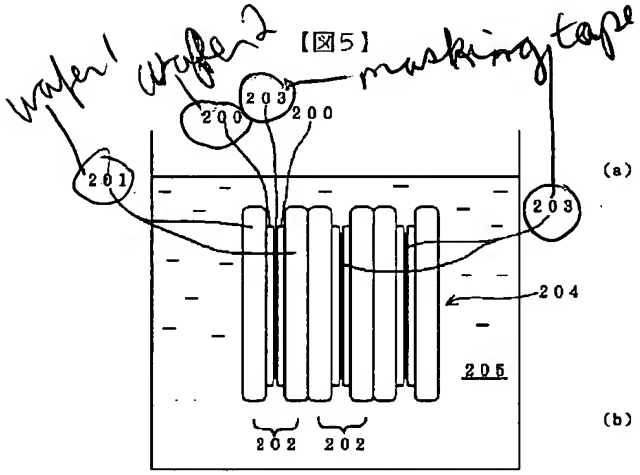
【図1】


1
2
1c
2a
面取り
1a
1
1b
表面（1b）仕上げ研磨
1c
1
張り合わせ
2
2a
1a
SOI
熱処理
1d
1
研　削
1a
2
2a
1
研　磨
1a
2
2a
SOI

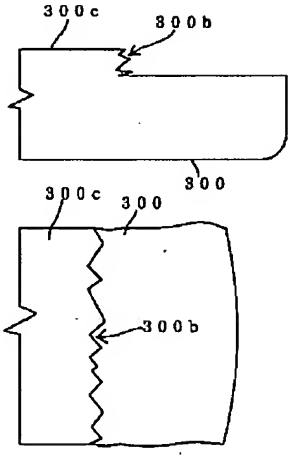
【図4】


100
104
104a
102
100a
a
101
101
103

【図5】


wafer1
wafer2
masking tape
203
200
200
201
203
204
205
202
202

【図7】


300c
300b
(a)
300
300c
300
300b
(b)

JP10-335195

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] In the manufacture approach of a lamination substrate of having made the wafer for support substrates, and the wafer for barrier layers rivaling The process which exposes the wafer periphery section on one side of the above-mentioned wafer for barrier layers, and prepares masking material in it, The process which the wafer for barrier layers which has this masking material is contacted to an etching reagent, and carries out etching beveling of the periphery section of above-mentioned wafer one side, The process which removes the above-mentioned masking material, and the field by the side of the above-mentioned beveling as a lamination side The above-mentioned wafer for barrier layers to the above-mentioned wafer for support substrates Lamination and the process heat-treated after that, The manufacture approach of the lamination substrate equipped with the process which carries out grinding of the front face of the wafer for barrier layers after the above-mentioned lamination until it reaches the beveling part of the above-mentioned wafer periphery section, and the process which grinds this grinding side.
[Claim 2] The manufacture approach of the lamination substrate according to claim 1 which carries out etching beveling by dipping each wafer periphery section in an etching reagent collectively, carrying out the laminating of two or more above-mentioned wafers for barrier layers one by one with superposition for these masking material, and rotating this layered product subsequently to focusing on a wafer axis after preparing the above-mentioned masking material.

[Translation done.]

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of lamination substrates, such as the manufacture approach of a lamination substrate, for example, a silicon-on silicon substrate, (direct lamination substrate), and a SOI (Silicon onInsulator) substrate which made the insulating layer intervene in between.
[0002]
[Description of the Prior Art] In manufacture of a SOI substrate, the room temperature is performing superposition and lamination heat treatment predetermined after that for the silicon wafer for support substrates, and the silicon wafer for barrier layers on both sides of the insulator layer (SiO2). Furthermore, in order to remove a poor lamination field, the periphery section of the wafer for barrier layers is beveled. Then, grinding of the front face of the wafer for barrier layers is carried out, and it is ground.
[0003] Beveling after this lamination specifically carries out grinding of the periphery section of the wafer for barrier layers by the wheel for beveling, etches this beveling side after that, and, usually a processing damage is removed. As the removal approach of this processing damage, as shown in drawing 4 , etching by dipping which carries out the gathers of many lamination substrates is known. By this gathers etching, the laminating of the lamination substrate 101 of predetermined number of sheets is carried out one by one with superposition for surface 100a of the wafer 100 for barrier layers. Then, each wafer periphery section is collectively dipped in an etching reagent 103, rotating this layered product 102 focusing on the wafer axis a. In beveling of the wafer periphery section after this lamination, when performing mechanical beveling using a wheel, there was a trouble that a processing damage also reached the side front of the wafer 104 for support substrates. In addition, drawing 4 is the explanatory view showing the etching process of the lamination substrate by gathers dipping which starts a means conventionally. In this drawing, 104 is a wafer for support substrates, and SiO2 film with which 104a was formed in the front face of the wafer 104 for support substrates.
[0004] Then, the "manufacture approach of a semiconductor device" of a publication is learned by JP,4-85827,A as a conventional technique which cancels this. This conventional approach performs mechanical beveling to the periphery section of the wafer for barrier layers before lamination by the wheel which is a grinding stone. In addition, after that, the field by the side of this beveling is made into a lamination side, and the wafer for barrier layers and the wafer for support substrates are given to the front face of the wafer for barrier layers for grinding, polish, etc. after lamination and predetermined heat treatment.
[0005] Moreover, "the junction wafer and its manufacture approach" which were indicated by JP,3-250616,A are learned as a conventional technique different from this. This another approach removes the periphery section of the wafer for barrier layers with etching beveling after lamination for wafers. It explains with reference to the explanatory view showing hereafter the etching process of the lamination substrate by gathers dipping which starts other conventional means of drawing 5 in this.

[0006] As this drawing is shown, the wafer 200 for barrier layers is made to rival to the wafer 201 for support substrates through SiO2 film in the middle, and the lamination substrate 202 is produced. In these lamination substrates 202, surface grinding of the wafer 200 for barrier layers is carried out, respectively. Then, a masking tape 203 is stuck on front faces other than the periphery section of each wafer 200 for barrier layers. next, the front faces of a masking tape 203 -- piling up -- these -- many -- the gathers of several lamination substrates 202 are carried out. Then, dipping of this layered product 204 is carried out to an etching reagent 205, and etching removal of the periphery section of each wafer 200 for barrier layers is carried out.

[0007]

[Problem(s) to be Solved by the Invention] However, there was following un-arranging by these conventional approaches. That is, although mechanical beveling by the wheel 301 is performed to the periphery section of the wafer 300 for barrier layers, usually the grinding side 301a of the wheel 301 for grinding is ruined [in the case] before the former lamination, as shown in drawing 6 with repeated beveling processing. As a result of mechanical beveling by such rough grinding side 301a, as shown in drawing 7 (a) and drawing 7 (b), inner circumference flank 300b of the beveling part of the wafer 300 for barrier layers became rude, and there was a possibility that a processing damage might arise on the periphery edge of surface 300c of the wafer 300 for barrier layers. Therefore, there was a trouble that a void occurred between wafers by considering this processing damage as a cause. Moreover, when the processing damage of the grinding produced in inner circumference flank 300b of the beveling part of the wafer 300 for barrier layers was comparatively serious, there was also a trouble that the slip resulting from this damage arose, at the time of heat treatment after lamination. In addition, similarly the explanatory view of the mechanical beveling process of the wafer periphery section for barrier layers which starts a means conventionally as for drawing 6 , the expanded sectional view of the periphery section of the wafer for barrier layers after mechanical beveling which relates to a means conventionally as for drawing 7 (a), and drawing 7 (b) are the expansion top views of the wafer periphery section.

[0008] On the other hand, as shown in drawing 5 , although etching beveling which used the masking tape 202 for the periphery section of the wafer 200 for barrier layers was performed, since etching removal not only of the periphery section of the wafer 200 for barrier layers but the periphery section of the wafer 201 for support substrates was carried out over the wafer thickness whole region, there was a trouble that the wafer 201 for support substrates minor-diameter-ized in a case after lamination.

[0009]

[Objects of the Invention] Then, this invention can improve the smooth nature in the periphery edge of the front face of the beveled wafer for barrier layers, and sets it as that purpose to offer the manufacture approach of the lamination substrate which can prevent void generating between wafers by this. Moreover, this invention sets it as that purpose to offer the manufacture approach of the lamination substrate which can prevent slip generating of the wafer for barrier layers which originated in the processing damage by beveling at the time of lamination heat treatment. Furthermore, this invention sets it as that purpose to offer the manufacture approach of a lamination substrate that minor diameter-ization of the wafer for support substrates by etching beveling does not break out. It sets it as the purpose to offer the manufacture approach of a pan and the lamination substrate which can mass-produce the wafer for barrier layers with which etching beveling of the periphery section was carried out.

[0010]

[Means for Solving the Problem] In the manufacture approach of a lamination substrate that invention according to claim 1 made the wafer for support substrates, and the wafer for barrier layers rival The process which exposes the wafer periphery section on one side of the above-mentioned wafer for barrier layers, and prepares masking material in it, The process which the wafer for barrier layers which has this masking material is contacted to an etching reagent, and carries out etching beveling of the periphery section of above-mentioned wafer one side, The process which removes the above-mentioned masking material, and the field by the side of the above-mentioned beveling as a lamination side The above-mentioned wafer for barrier layers to the above-mentioned wafer for support substrates Lamination and the process heat-treated after that, It is the manufacture approach of the lamination substrate equipped

with the process which carries out grinding of the front face of the wafer for barrier layers after the above-mentioned lamination until it reaches the beveling part of the above-mentioned wafer periphery section, and the process which grinds this grinding side.

[0011] The coat which consists of a masking tape which consists of synthetic resin, such as Teflon (trade name; fluororesin) and polyethylene, a wax, other macromolecule organic compounds excellent in corrosion resistance, etc. is sufficient as masking material here. The thickness of masking material has desirable 80 micrometers or more, and in less than 80 micrometers, for example, masking material is piled up, a layered product is formed, each wafer periphery section of this is put in block, and in case it dips in an etching reagent and etching beveling is carried out, this etching reagent cannot enter easily to the clearance between the periphery sections of the adjoining wafer for barrier layers. Moreover, it says making etching beveling here **** the periphery section of the wafer for barrier layers with which only predetermined time (HF/HNO3 for 3 - 5 minutes) contacts for example, the wafer for barrier layers, and it is not covered by masking material by this in etching reagents, such as a mixed acid which mixed fluoric acid and a nitric acid, a potassium hydroxide, or a sodium hydroxide, only for the specified quantity.

[0012] Furthermore, the thickness by desirable etching beveling of the periphery section of the wafer for barrier layers is 1/2 of the thickness of 50 micrometers - a wafer. In less than 50 micrometers, there is a possibility of damaging the front-face side of the periphery section of the wafer for support substrates, at the time of the surface grinding of the wafer for barrier layers after the lamination of the wafer for barrier layers, and the wafer for support substrates. On the other hand, when it exceeds one half of wafer thickness, there is a possibility that the mechanical strength of the wafer periphery section may fall sharply.

[0013] Especially the radial etching beveling width of face of the periphery section of the wafer for barrier layers has 1-3 desirablemm 0.8-5.0mm. less than 0.8mm -- periphery polish of each wafer -- the poor junction resulting from whom becomes easy to occur. Moreover, if it exceeds 5.0mm, the effective area in a wafer will become small. Moreover, the grinding thickness of the front face of the wafer for barrier layers after lamination is not limited that what is necessary is just to have reached the beveling part at least.

[0014] Furthermore, the wafer for barrier layers may perform surface-finish polish of a lamination side, before being stretched by the wafer for support substrates. Surface-finish polish here means polish of less than 0.1 micrometers by the non-wax polishing of surface criteria. After surface-finish polish of the wafer for barrier layers usually washes the front face of the wafer for barrier layers by SC1 (Standard Cleaning1), SC1+ dilute hydrochloric acid, SC1+HCl/HF, SC1+HF, etc. In addition, as a wafer for barrier layers, the front face may be covered with SiO2 film. Moreover, this SiO2 film may be prepared in the wafer for barrier layers at any process among the production process of a lamination substrate.

[0015] It is the manufacture approach of the lamination substrate according to claim 1 which carries out etching beveling by dipping each wafer periphery section in an etching reagent collectively, it carrying out the laminating of two or more above-mentioned wafers for barrier layers one by one with superposition for these masking material, and rotating this layered product subsequently to focusing on a wafer axis, after invention according to claim 2 prepares the above-mentioned masking material. The laminating number of sheets and rotational speed of the wafer for barrier layers are fundamentally the same as the conventional approach which carries out the gathers of many lamination substrates, and is etched by dipping. In addition, even if it does not perform etching beveling of the wafer for barrier layers by putting two or more sheets in block in this way, it is good at a time in a line. [of one sheet]

[0016]

[Function] According to this invention, before making the wafer for support substrates rival, beforehand, the wafer periphery section is exposed on one side of the wafer for barrier layers, masking material is prepared in it, the wafer for barrier layers with this masking material is dipped in an etching reagent after that, and the periphery section of one side of the wafer for barrier layers is beveled by etching. Subsequently, the field by the side of beveling is made into a lamination side, and the wafer for barrier layers and the wafer for support substrates are heat-treated lamination and after that. And grinding of the

front face of the wafer for barrier layers after lamination is carried out until it reaches a beveling part, this grinding side is ground further, and a lamination substrate is manufactured.

[0017] In beveling of the wafer periphery section in the former, mechanical beveling after lamination (beveling with a grinding stone) and etching beveling was adopted. Consequently, the front-face side of the periphery section of the wafer for support substrates was damaged with this grinding stone, or a part of periphery section of the wafer for support substrates melted into the etching reagent, and there was a possibility that minor diameter-ization of the wafer for support substrates by etching beveling might arise. However, since the wafer periphery section is beveled before lamination in this invention, such fear does not exist.

[0018] Moreover, in the case of conventional mechanical beveling, grinding of the inner circumference flank of the chamfer in the wafer for barrier layers is carried out in respect of the grinding it was usually ruined with repeated use of the wheel which is a grinding stone. For this reason, in the periphery edge of the front face of the beveled wafer for barrier layers, the processing damage resulting from mechanical beveling occurred. however -- since it dips in an etching reagent and bevels in this invention, without using a wheel -- such a processing damage -- not generating -- consequently, the front face of the wafer for barrier layers -- the smooth nature to kick can be improved. Moreover, since this beveling is beveling by etching, in the time of lamination heat treatment, slip generating of the wafer for barrier layers resulting from the processing damage by beveling can be prevented.

[0019] Especially, according to invention according to claim 2, masking material is prepared in one side of the wafer for barrier layers which has two or more sheets first, respectively. Then, masking material is piled up and the laminating of the wafer for barrier layers is carried out one by one. Subsequently, etching beveling of this part is carried out by putting each wafer periphery section in block, dipping in an etching reagent or carrying out the spray of the etching reagent, rotating this layered product focusing on a wafer axis. Consequently, the periphery section can mass-produce comparatively easily the wafer for barrier layers by which etching beveling was carried out. Moreover, peeling of the masking material for etching can also be lost completely.

[0020]

[Embodiment of the Invention] Hereafter, the example of this invention is explained with reference to a drawing. In addition, a SOI substrate is explained to an example as a lamination substrate here. Drawing 1 is the flow sheet of the manufacture approach of the lamination substrate concerning one example of this invention. Drawing 2 is the explanatory view showing the etching beveling process of the periphery section of the wafer for barrier layers. Drawing 3 is the enlarged drawing of the wafer for barrier layers immediately after etching beveling.

[0021] According to this example, as shown in drawing 1 , the wafer 1 (mirror-polishing wafer) for barrier layers made from silicon is prepared beforehand. Moreover, oxide-film (SiO2) 2a which is an insulator layer is formed in the front face of the same material as the wafer 1 for barrier layers, and the wafer 2 (mirror-polishing wafer) for support substrates of the same aperture. Next, 100 micrometers only in 3mm and thickness carry out etching beveling of the periphery section of the wafer 1 for barrier layers from a front-face side to the wafer radial.

[0022] This etching beveling is explained with reference to drawing 2 . Where the wafer periphery section is exposed, the masking material 3 which consists of a masking tape "BT-50E" by NITTO DENKO CORP. of a small-circle plate from this wafer 1 is stuck on the front face of this wafer 1 for barrier layers. Then, the laminating of two or more wafers 1 for barrier layers is carried out for masking material 3 comrades one by one with superposition, and a layered product 4 is formed. Subsequently, rotating a layered product 4 at a predetermined rate focusing on the wafer axis a, the wafer periphery section of each wafer 1 for barrier layers is put in block, it is immersed in the etching reagent 5 of HF/HNO3, and etching beveling is carried out.

[0023] As shown in drawing 3 , the wafer periphery section of the wafer 1 for barrier layers ****(ed) only thickness t (here 100 micrometers) with this etching beveling. In addition, this **** attains to the whole periphery section of the wafer 1 for barrier layers (refer to drawing 3 two-dot chain line). Thus, since the periphery section of the wafer 1 for barrier layers is beveled before lamination, there is no

possibility of damaging the front-face side of the periphery section of the wafer 2 for support substrates with a grinding stone, like [in mechanical beveling after the lamination in the conventional technique]. Both, the periphery section of the wafer 2 for support substrates melts at the time of etching, and this wafer 2 does not minor-diameter-ize. And since the processing damage resulting from mechanical beveling has not arisen in the periphery edge of the front face of the beveled wafer for barrier layers, the smooth nature in the front face of the wafer for barrier layers can be improved. Furthermore, in the time of lamination heat treatment, a slip of the wafer 1 for barrier layers resulting from the processing damage by beveling can be prevented.

[0024] Then, the masking material 3 is removed. Next, as shown in drawing 1 , finishing polish of the surface 1b of the wafer 1 for barrier layers in front of lamination is carried out. Finishing polish is polish of less than 0.1 micrometers by the wax loess mounting method of surface criteria. After polish washes the front face of this wafer for barrier layers. Usually, it is based on SC1 washing, SC1 washing + dilute-hydrochloric-acid washing, SC1 washing +HF washing, or SC1 washing +HCl/HF washing.

[0025] Subsequently, the wafer 1 for barrier layers and the wafer 2 for support substrates are made for surface 1b by the side of beveling to rival at a room temperature as a lamination side. Furthermore, predetermined lamination heat treatment is performed (for example, 1100 degrees C, 2 hours). Consequently, the wafer 1 for barrier layers will be stretched through oxide-film 2a by the wafer 2 for support substrates. Then, rough grinding is carried out by the wheel outside drawing which has the abrasive grain of comparatively the low yarn count until it reaches a beveling part from the surface 1c side in the wafer 1 for barrier layers. Subsequently, thin grinding is carried out by the wheel which has the abrasive grain of comparatively the high yarn count until the remaining thickness of the periphery section of the wafer 1 for barrier layers becomes +5 micrometers in purpose thickness. Subsequently, 1d only of 5 micrometers of front faces after this surface grinding is ground. The SOI substrate with which the barrier layer of given thickness (for example, 10 micrometers) was arranged through insulator layer 2a on the wafer 2 for support substrates by this is obtained.

[0026]

[Effect of the Invention] Since it was made to carry out etching beveling of the periphery section which is not covered with the masking material of one side of the wafer for barrier layers in front of lamination with the wafer for support substrates according to the manufacture approach of the lamination substrate concerning this invention, while a possibility may damage the front-face side of the periphery section of the wafer for support substrates which serves as the base at the time of beveling disappears, minor diameter-ization of the wafer for support substrates by etching beveling does not occur. And in the periphery edge of the front face of the beveled wafer for barrier layers, the processing damage resulting from mechanical beveling does not arise. Consequently, the smooth nature in the front face of the wafer for barrier layers can be improved. Furthermore, slip generating of the wafer for barrier layers which originated in the processing damage of this mechanical beveling part at the time of lamination heat treatment can also be prevented. And since masking material is stuck and etched on a wafer front face before lamination, a routing counter does not increase and productive efficiency can be raised.

[0027] Since each wafer periphery section is collectively dipped especially in an etching reagent, rotating the layered product which was obtained by piling up masking material and carrying out the laminating of two or more wafers for barrier layers with masking material one by one according to invention according to claim 2 focusing on a wafer axis and it was made to carry out etching beveling, the wafer for barrier layers with which etching beveling of the periphery section was carried out can be mass-produced comparatively easily.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of lamination substrates, such as the manufacture approach of a lamination substrate, for example, a silicon-on silicon substrate, (direct lamination substrate), and a SOI (Silicon onInsulator) substrate which made the insulating layer intervene in between.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] In manufacture of a SOI substrate, the room temperature is performing superposition and lamination heat treatment predetermined after that for the silicon wafer for support substrates, and the silicon wafer for barrier layers on both sides of the insulator layer (SiO2). Furthermore, in order to remove a poor lamination field, the periphery section of the wafer for barrier layers is beveled. Then, grinding of the front face of the wafer for barrier layers is carried out, and it is ground.
[0003] Beveling after this lamination specifically carries out grinding of the periphery section of the wafer for barrier layers by the wheel for beveling, etches this beveling side after that, and, usually a processing damage is removed. As the removal approach of this processing damage, as shown in drawing 4 , etching by dipping which carries out the gathers of many lamination substrates is known. By this gathers etching, the laminating of the lamination substrate 101 of predetermined number of sheets is carried out one by one with superposition for surface 100a of the wafer 100 for barrier layers. Then, each wafer periphery section is collectively dipped in an etching reagent 103, rotating this layered product 102 focusing on the wafer axis a. In beveling of the wafer periphery section after this lamination, when performing mechanical beveling using a wheel, there was a trouble that a processing damage also reached the side front of the wafer 104 for support substrates. In addition, drawing 4 is the explanatory view showing the etching process of the lamination substrate by gathers dipping which starts a means conventionally. In this drawing, 104 is a wafer for support substrates, and SiO2 film with which 104a was formed in the front face of the wafer 104 for support substrates.
[0004] Then, the "manufacture approach of a semiconductor device" of a publication is learned by JP,4-85827,A as a conventional technique which cancels this. This conventional approach performs mechanical beveling to the periphery section of the wafer for barrier layers before lamination by the wheel which is a grinding stone. In addition, after that, the field by the side of this beveling is made into a lamination side, and the wafer for barrier layers and the wafer for support substrates are given to the front face of the wafer for barrier layers for grinding, polish, etc. after lamination and predetermined heat treatment.
[0005] Moreover, "the junction wafer and its manufacture approach" which were indicated by JP,3-250616,A are learned as a conventional technique different from this. This another approach removes the periphery section of the wafer for barrier layers with etching beveling after lamination for wafers. It explains with reference to the explanatory view showing hereafter the etching process of the lamination substrate by gathers dipping which starts other conventional means of drawing 5 in this.
[0006] As this drawing is shown, the wafer 200 for barrier layers is made to rival to the wafer 201 for support substrates through SiO2 film in the middle, and the lamination substrate 202 is produced. In these lamination substrates 202, surface grinding of the wafer 200 for barrier layers is carried out, respectively. Then, a masking tape 203 is stuck on front faces other than the periphery section of each wafer 200 for barrier layers. next, the front faces of a masking tape 203 -- piling up -- these -- many -- the gathers of several lamination substrates 202 are carried out. Then, dipping of this layered product 204 is carried out to an etching reagent 205, and etching removal of the periphery section of each wafer

200 for barrier layers is carried out.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] Since it was made to carry out etching beveling of the periphery section which is not covered with the masking material of one side of the wafer for barrier layers in front of lamination with the wafer for support substrates according to the manufacture approach of the lamination substrate concerning this invention, while a possibility may damage the front-face side of the periphery section of the wafer for support substrates which serves as the base at the time of beveling disappears, minor diameter-ization of the wafer for support substrates by etching beveling does not occur. And in the periphery edge of the front face of the beveled wafer for barrier layers, the processing damage resulting from mechanical beveling does not arise. Consequently, the smooth nature in the front face of the wafer for barrier layers can be improved. Furthermore, slip generating of the wafer for barrier layers which originated in the processing damage of this mechanical beveling part at the time of lamination heat treatment can also be prevented. And since masking material is stuck and etched on a wafer front face before lamination, a routing counter does not increase and productive efficiency can be raised.
[0027] Since each wafer periphery section is collectively dipped especially in an etching reagent, rotating the layered product which was obtained by piling up masking material and carrying out the laminating of two or more wafers for barrier layers with masking material one by one according to invention according to claim 2 focusing on a wafer axis and it was made to carry out etching beveling, the wafer for barrier layers with which etching beveling of the periphery section was carried out can be mass-produced comparatively easily.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, there was following un-arranging by these conventional approaches. That is, although mechanical beveling by the wheel 301 is performed to the periphery section of the wafer 300 for barrier layers, usually the grinding side 301a of the wheel 301 for grinding is ruined [in the case] before the former lamination, as shown in drawing 6 with repeated beveling processing. As a result of mechanical beveling by such rough grinding side 301a, as shown in drawing 7 (a) and drawing 7 (b), inner circumference flank 300b of the beveling part of the wafer 300 for barrier layers became rude, and there was a possibility that a processing damage might arise on the periphery edge of surface 300c of the wafer 300 for barrier layers. Therefore, there was a trouble that a void occurred between wafers by considering this processing damage as a cause. Moreover, when the processing damage of the grinding produced in inner circumference flank 300b of the beveling part of the wafer 300 for barrier layers was comparatively serious, there was also a trouble that the slip resulting from this damage arose, at the time of heat treatment after lamination. In addition, similarly the explanatory view of the mechanical beveling process of the wafer periphery section for barrier layers which starts a means conventionally as for drawing 6 , the expanded sectional view of the periphery section of the wafer for barrier layers after mechanical beveling which relates to a means conventionally as for drawing 7 (a), and drawing 7 (b) are the expansion top views of the wafer periphery section.
[0008] On the other hand, as shown in drawing 5 , although etching beveling which used the masking tape 202 for the periphery section of the wafer 200 for barrier layers was performed, since etching removal not only of the periphery section of the wafer 200 for barrier layers but the periphery section of the wafer 201 for support substrates was carried out over the wafer thickness whole region, there was a trouble that the wafer 201 for support substrates minor-diameter-ized in a case after lamination.
[0009]
[Objects of the Invention] Then, this invention can improve the smooth nature in the periphery edge of the front face of the beveled wafer for barrier layers, and sets it as that purpose to offer the manufacture approach of the lamination substrate which can prevent void generating between wafers by this. Moreover, this invention sets it as that purpose to offer the manufacture approach of the lamination substrate which can prevent slip generating of the wafer for barrier layers which originated in the processing damage by beveling at the time of lamination heat treatment. Furthermore, this invention sets it as that purpose to offer the manufacture approach of a lamination substrate that minor diameter-ization of the wafer for support substrates by etching beveling does not break out. It sets it as the purpose to offer the manufacture approach of a pan and the lamination substrate which can mass-produce the wafer for barrier layers with which etching beveling of the periphery section was carried out.

[Translation done.]

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MEANS

[Means for Solving the Problem] In the manufacture approach of a lamination substrate that invention according to claim 1 made the wafer for support substrates, and the wafer for barrier layers rival The process which exposes the wafer periphery section on one side of the above-mentioned wafer for barrier layers, and prepares masking material in it, The process which the wafer for barrier layers which has this masking material is contacted to an etching reagent, and carries out etching beveling of the periphery section of above-mentioned wafer one side, The process which removes the above-mentioned masking material, and the field by the side of the above-mentioned beveling as a lamination side The above-mentioned wafer for barrier layers to the above-mentioned wafer for support substrates Lamination and the process heat-treated after that, It is the manufacture approach of the lamination substrate equipped with the process which carries out grinding of the front face of the wafer for barrier layers after the above-mentioned lamination until it reaches the beveling part of the above-mentioned wafer periphery section, and the process which grinds this grinding side.
[0011] The coat which consists of a masking tape which consists of synthetic resin, such as Teflon (trade name; fluororesin) and polyethylene, a wax, other macromolecule organic compounds excellent in corrosion resistance, etc. is sufficient as masking material here. The thickness of masking material has desirable 80 micrometers or more, and in less than 80 micrometers, for example, masking material is piled up, a layered product is formed, each wafer periphery section of this is put in block, and in case it dips in an etching reagent and etching beveling is carried out, this etching reagent cannot enter easily to the clearance between the periphery sections of the adjoining wafer for barrier layers. Moreover, it says making etching beveling here **** the periphery section of the wafer for barrier layers with which only predetermined time (HF/HNO3 for 3 - 5 minutes) contacts for example, the wafer for barrier layers, and it is not covered by masking material by this in etching reagents, such as a mixed acid which mixed fluoric acid and a nitric acid, a potassium hydroxide, or a sodium hydroxide, only for the specified quantity.
[0012] Furthermore, the thickness by desirable etching beveling of the periphery section of the wafer for barrier layers is 1/2 of the thickness of 50 micrometers - a wafer. In less than 50 micrometers, there is a possibility of damaging the front-face side of the periphery section of the wafer for support substrates, at the time of the surface grinding of the wafer for barrier layers after the lamination of the wafer for barrier layers, and the wafer for support substrates. On the other hand, when it exceeds one half of wafer thickness, there is a possibility that the mechanical strength of the wafer periphery section may fall sharply.
[0013] Especially the radial etching beveling width of face of the periphery section of the wafer for barrier layers has 1-3 desirablemm 0.8-5.0mm. less than 0.8mm -- periphery polish of each wafer -- the poor junction resulting from whom becomes easy to occur. Moreover, if it exceeds 5.0mm, the effective area in a wafer will become small. Moreover, the grinding thickness of the front face of the wafer for barrier layers after lamination is not limited that what is necessary is just to have reached the beveling part at least.
[0014] Furthermore, the wafer for barrier layers may perform surface-finish polish of a lamination side,

before being stretched by the wafer for support substrates. Surface-finish polish here means polish of less than 0.1 micrometers by the non-wax polishing of surface criteria. After surface-finish polish of the wafer for barrier layers usually washes the front face of the wafer for barrier layers by SC1 (Standard Cleaning1), SC1+dilute hydrochloric acid, SC1+HCl/HF, SC1+HF, etc. In addition, as a wafer for barrier layers, the front face may be covered with SiO2 film. Moreover, this SiO2 film may be prepared in the wafer for barrier layers at any process among the production process of a lamination substrate. [0015] It is the manufacture approach of the lamination substrate according to claim 1 which carries out etching beveling by dipping each wafer periphery section in an etching reagent collectively, it carrying out the laminating of two or more above-mentioned wafers for barrier layers one by one with superposition for these masking material, and rotating this layered product subsequently to focusing on a wafer axis, after invention according to claim 2 prepares the above-mentioned masking material. The laminating number of sheets and rotational speed of the wafer for barrier layers are fundamentally the same as the conventional approach which carries out the gathers of many lamination substrates, and is etched by dipping. In addition, even if it does not perform etching beveling of the wafer for barrier layers by putting two or more sheets in block in this way, it is good at a time in a line. [of one sheet]

[Translation done.]

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OPERATION

[Function] According to this invention, before making the wafer for support substrates rival, beforehand, the wafer periphery section is exposed on one side of the wafer for barrier layers, masking material is prepared in it, the wafer for barrier layers with this masking material is dipped in an etching reagent after that, and the periphery section of one side of the wafer for barrier layers is beveled by etching. Subsequently, the field by the side of beveling is made into a lamination side, and the wafer for barrier layers and the wafer for support substrates are heat-treated lamination and after that. And grinding of the front face of the wafer for barrier layers after lamination is carried out until it reaches a beveling part, this grinding side is ground further, and a lamination substrate is manufactured.
[0017] In beveling of the wafer periphery section in the former, mechanical beveling after lamination (beveling with a grinding stone) and etching beveling was adopted. Consequently, the front-face side of the periphery section of the wafer for support substrates was damaged with this grinding stone, or a part of periphery section of the wafer for support substrates melted into the etching reagent, and there was a possibility that minor diameter-ization of the wafer for support substrates by etching beveling might arise. However, since the wafer periphery section is beveled before lamination in this invention, such fear does not exist.
[0018] Moreover, in the case of conventional mechanical beveling, grinding of the inner circumference flank of the chamfer in the wafer for barrier layers is carried out in respect of the grinding it was usually ruined with repeated use of the wheel which is a grinding stone. For this reason, in the periphery edge of the front face of the beveled wafer for barrier layers, the processing damage resulting from mechanical beveling occurred. however -- since it dips in an etching reagent and bevels in this invention, without using a wheel -- such a processing damage -- not generating -- consequently, the front face of the wafer for barrier layers -- the smooth nature to kick can be improved. Moreover, since this beveling is beveling by etching, in the time of lamination heat treatment, slip generating of the wafer for barrier layers resulting from the processing damage by beveling can be prevented.
[0019] Especially, according to invention according to claim 2, masking material is prepared in one side of the wafer for barrier layers which has two or more sheets first, respectively. Then, masking material is piled up and the laminating of the wafer for barrier layers is carried out one by one. Subsequently, etching beveling of this part is carried out by putting each wafer periphery section in block, dipping in an etching reagent or carrying out the spray of the etching reagent, rotating this layered product focusing on a wafer axis. Consequently, the periphery section can mass-produce comparatively easily the wafer for barrier layers by which etching beveling was carried out. Moreover, peeling of the masking material for etching can also be lost completely.
[0020]
[Embodiment of the Invention] Hereafter, the example of this invention is explained with reference to a drawing. In addition, a SOI substrate is explained to an example as a lamination substrate here. Drawing 1 is the flow sheet of the manufacture approach of the lamination substrate concerning one example of this invention. Drawing 2 is the explanatory view showing the etching beveling process of the periphery section of the wafer for barrier layers. Drawing 3 is the enlarged drawing of the wafer for barrier layers

immediately after etching beveling.
[0021] According to this example, as shown in drawing 1 , the wafer 1 (mirror-polishing wafer) for barrier layers made from silicon is prepared beforehand. Moreover, oxide-film (SiO2) 2a which is an insulator layer is formed in the front face of the same material as the wafer 1 for barrier layers, and the wafer 2 (mirror-polishing wafer) for support substrates of the same aperture. Next, 100 micrometers only in 3mm and thickness carry out etching beveling of the periphery section of the wafer 1 for barrier layers from a front-face side to the wafer radial.
[0022] This etching beveling is explained with reference to drawing 2 . Where the wafer periphery section is exposed, the masking material 3 which consists of a masking tape "BT-50E" by NITTO DENKO CORP. of a small-circle plate from this wafer 1 is stuck on the front face of this wafer 1 for barrier layers. Then, the laminating of two or more wafers 1 for barrier layers is carried out for masking material 3 comrades one by one with superposition, and a layered product 4 is formed. Subsequently, rotating a layered product 4 at a predetermined rate focusing on the wafer axis a, the wafer periphery section of each wafer 1 for barrier layers is put in block, it is immersed in the etching reagent 5 of HF/HNO3, and etching beveling is carried out.
[0023] As shown in drawing 3 , the wafer periphery section of the wafer 1 for barrier layers ****(ed) only thickness t (here 100 micrometers) with this etching beveling. In addition, this **** attains to the whole periphery section of the wafer 1 for barrier layers (refer to drawing 3 two-dot chain line). Thus, since the periphery section of the wafer 1 for barrier layers is beveled before lamination, there is no possibility of damaging the front-face side of the periphery section of the wafer 2 for support substrates with a grinding stone, like [in mechanical beveling after the lamination in the conventional technique]. Both, the periphery section of the wafer 2 for support substrates melts at the time of etching, and this wafer 2 does not minor-diameter-ize. And since the processing damage resulting from mechanical beveling has not arisen in the periphery edge of the front face of the beveled wafer for barrier layers, the smooth nature in the front face of the wafer for barrier layers can be improved. Furthermore, in the time of lamination heat treatment, a slip of the wafer 1 for barrier layers resulting from the processing damage by beveling can be prevented.
[0024] Then, the masking material 3 is removed. Next, as shown in drawing 1 , finishing polish of the surface 1b of the wafer 1 for barrier layers in front of lamination is carried out. Finishing polish is polish of less than 0.1 micrometers by the wax loess mounting method of surface criteria. After polish washes the front face of this wafer for barrier layers. Usually, it is based on SC1 washing, SC1 washing + dilute-hydrochloric-acid washing, SC1 washing +HF washing, or SC1 washing +HCl/HF washing.
[0025] Subsequently, the wafer 1 for barrier layers and the wafer 2 for support substrates are made for surface 1b by the side of beveling to rival at a room temperature as a lamination side. Furthermore, predetermined lamination heat treatment is performed (for example, 1100 degrees C, 2 hours). Consequently, the wafer 1 for barrier layers will be stretched through oxide-film 2a by the wafer 2 for support substrates. Then, rough grinding is carried out by the wheel outside drawing which has the abrasive grain of comparatively the low yarn count until it reaches a beveling part from the surface 1c side in the wafer 1 for barrier layers. Subsequently, thin grinding is carried out by the wheel which has the abrasive grain of comparatively the high yarn count until the remaining thickness of the periphery section of the wafer 1 for barrier layers becomes +5 micrometers in purpose thickness. Subsequently, 1d only of 5 micrometers of front faces after this surface grinding is ground. The SOI substrate with which the barrier layer of given thickness (for example, 10 micrometers) was arranged through insulator layer 2a on the wafer 2 for support substrates by this is obtained.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the flow sheet which shows the outline of the manufacture approach of the lamination substrate concerning one example of this invention.
[Drawing 2] It is the explanatory view showing the etching beveling process of the periphery section of the wafer for barrier layers concerning one example of this invention.
[Drawing 3] It is the explanatory view showing the etching beveling process of the periphery section of the wafer for barrier layers concerning one example of this invention.
[Drawing 4] It is the explanatory view showing the etching process of the lamination substrate by gathers dipping which starts a means conventionally.
[Drawing 5] It is the explanatory view showing the etching process of the lamination substrate by gathers dipping concerning other conventional means.
[Drawing 6] It is the explanatory view of the mechanical beveling process of the wafer periphery section for barrier layers which starts a means conventionally.
[Drawing 7] (a) is the expanded sectional view of the periphery section of the wafer for barrier layers after mechanical beveling which relates to a means conventionally. Similarly (b) is the expansion top view of the wafer periphery section.
[Description of Notations]
1 Wafer for Barrier Layers,
2 Wafer for Support Substrates,
3 Masking Material,
4 Layered Product,
5 Etching Reagent,
Wafer axis.

[Translation done.]

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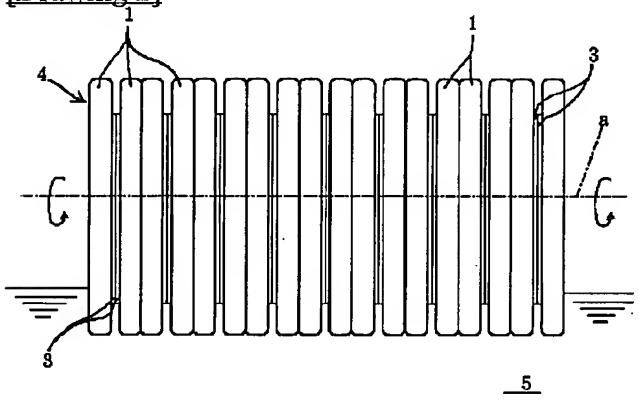
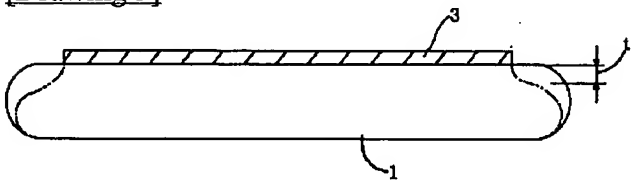
DRAWINGS

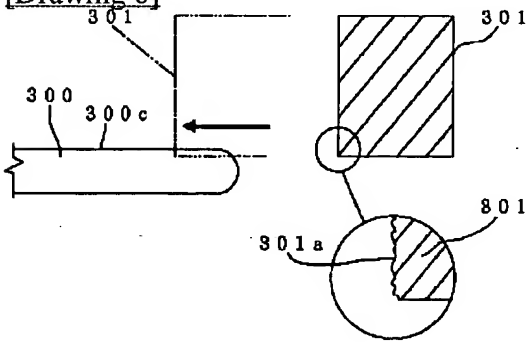
[Drawing 2]



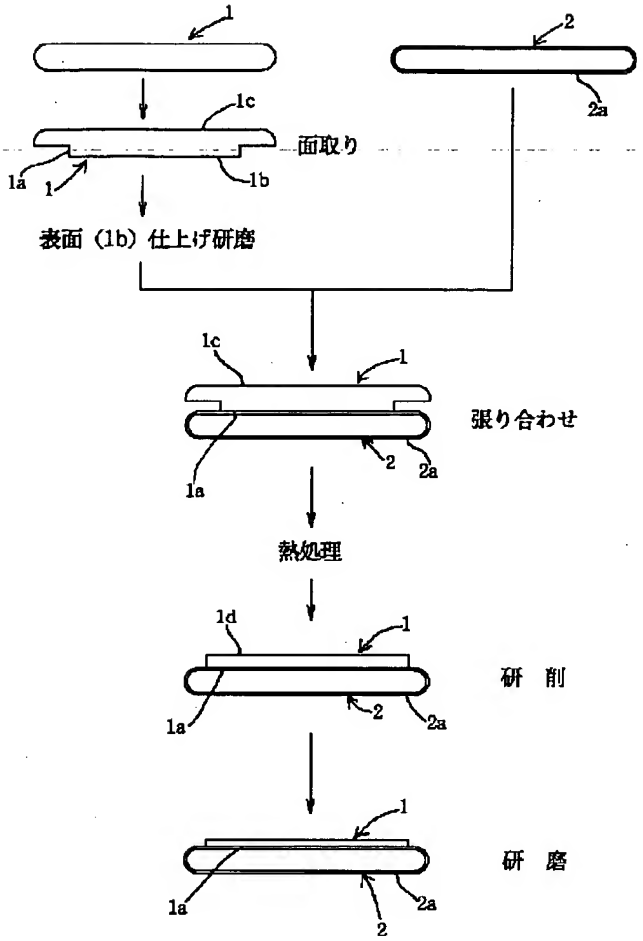
[Drawing 3]



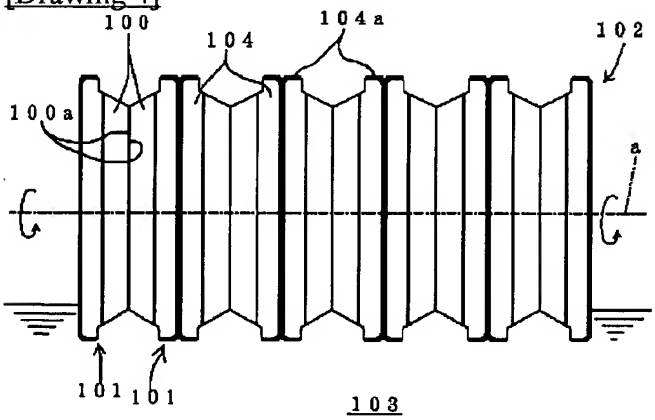
[Drawing 6]



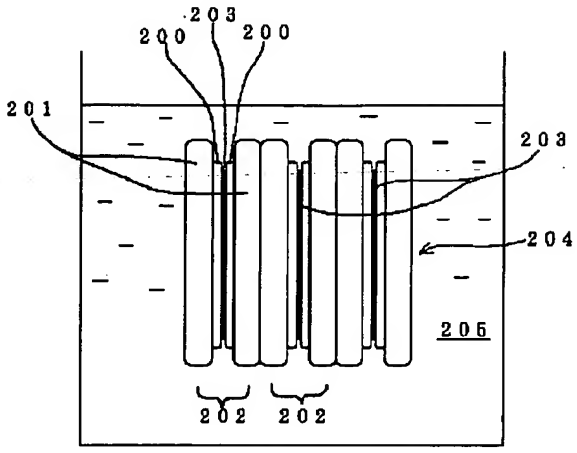
[Drawing 1]



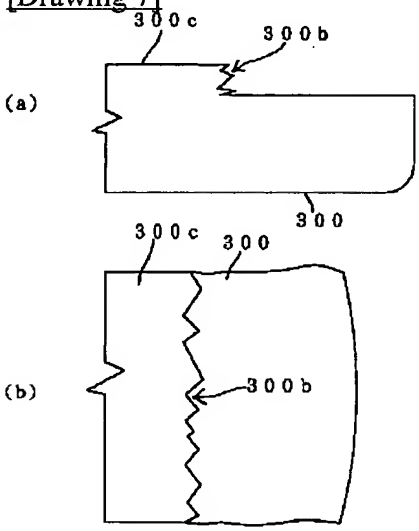
[Drawing 4]



[Drawing 5]



[Drawing 7]



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